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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,368	11/19/2003	David Walter Flynn	550-489	9185

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EXAMINER	
BROWN, MICHAEL J	

ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
11/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,368	FLYNN, DAVID WALTER	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8 and 11* is/are rejected.

7)☐ Claim(s) *4,5,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reexamination

1. In view of the Appeal Brief filed on 8/11/2008, PROSECUTION IS HEREBY REOPENED. As set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

***.

Allowable Subject Matter

2. Claims 4, 5, 9, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6-8, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Clark et al.[Clark](US Patent 6,519,707).

As to claim 1, Clark discloses an apparatus for processing data, said apparatus comprising a processor(processor 110, see Fig. 1) operable to perform data processing operations, said processor being operable to generate a performance control signal(binary digital signals; see column 4, line 61) indicative of a desired data processing performance level(frequency desirable to complete the specific microprocessor application in real time; see column 5, lines 29-30) of said processor; and at least one further circuit(control register 125, see Fig. 1) responsive to said performance control signal to operate so as to support said desired data processing performance level of said processor(see column 6, lines 7-10); wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level(adjusting the operating voltage of processor 110 up and/or down; see

column 5, lines 43-44), said at least one further circuit is operable to support data processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change(microprocessor may continue operating while the operating voltage level is varied; see column 7, lines 25-26, 42-45, and column 9, lines 1-3).

As to claim 2, Clark discloses the apparatus as claimed in claim 1, wherein said one or more further circuits include a voltage controller(voltage regulator 120, see Fig. 1) operable to generate a power signal for said processor at a plurality of different voltage levels(see column 5, lines 26-30).

As to claim 3, Clark discloses the apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator(PPL reference clock; see column 7, line 41) operable to generate a clock signal with a selectable clock frequency(see column 7, lines 39-45).

As to claim 6, Clark discloses a method of processing data, said method comprising the steps of performing data processing operations with a processor(processor 110, see Fig. 1), said processor being operable to generate a performance control signal(binary digital signals; see column 4, line 61) indicative of a desired data processing performance level(frequency desirable to complete the specific microprocessor application in real time; see column 5, lines 29-30) of said processor; and in response to said performance control signal, operating one or more further circuits(control register 125, see Fig. 1) so as to support said desired data processing

performance level of said processor(see column 6, lines 7-10); wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level(adjusting the operating voltage of processor 110 up and/or down; see column 5, lines 43-44), said one or more further circuits are operable to support data processing at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change(microprocessor may continue operating while the operating voltage level is varied; see column 7, lines 25-26, 42-45, and column 9, lines 1-3).

As to claim 7, Clark discloses the method as claimed in claim 6, wherein said one or more further circuits include a voltage controller(voltage regulator 120, see Fig. 1) operable to generate a power signal for said processor at a plurality of different voltage levels(see column 5, lines 26-30).

As to claim 8, Clark discloses the method as claimed in claim 6, wherein said one or more further circuits include a clock generator(PPL reference clock; see column 7, line 41) operable to generate a clock signal with a selectable clock frequency(see column 7, lines 39-45).

As to claim 11, Clark discloses an apparatus for processing data, said apparatus comprising a processor(processor 110, see Fig. 1) operable to perform data processing operations, said processor being operable to generate a performance control signal(binary digital signals; see column 4, line 61) indicative of a desired data

processing performance level(frequency desirable to complete the specific microprocessor application in real time; see column 5, lines 29-30) of said processor; and at least one further circuit(control register 125, see Fig. 1), responsive to said performance control signal, for supporting said desired data processing performance level of said processor(see column 6, lines 7-10); wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level(adjusting the operating voltage of processor 110 up and/or down; see column 5, lines 43-44), said at least one further circuit comprising a means for supporting data processing of said processor at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change(microprocessor may continue operating while the operating voltage level is varied; see column 7, lines 25-26, 42-45, and column 9, lines 1-3).

Response to Arguments

4. Applicant's arguments, see Appeal Brief, filed 8/11/2008, with respect to the rejection(s) of claim(s) 1-11 under 35 U.S.C. 103(a) as being unpatentable over Cooper(US Patent 6,823,516) in view of Tobias et al.(US Patent 7,254,721) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of

claims 1-3, 6-8, and 11 being rejected under 35 U.S.C. 102(e) as being anticipated by Clark et al.[Clark](US Patent 6,519,707).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Brown whose telephone number is (571)272-5932. The examiner can normally be reached Monday-Thursday from 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached at (571)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Brown/
Examiner, Art Unit 2116

/Thomas Lee/
Supervisory Patent Examiner, Art Unit 2115